Claim Amendments

Applicant has amended claim 1, cancelled claims 2-3, and added new claim 4. Applicant sets forth a complete listing of the claims with the corresponding status indicated for each claim.

1. (Currently Amended) A ~~spread spectrum~~ system for generating a reduced amplitude clock pulse ~~from an original primary clock pulse~~, the system comprising:

a clock signal generator for creating a ~~series of~~ clock signal ~~pulses~~;

~~a non-delayed line adapted to receive the series of clock pulses from the clock signal generator~~;

a delay line ~~comprising a delay time and~~ adapted to ~~cause a~~ receive the clock signal ~~transmitted to the delay line to be outputted after passage of the delay time~~ and to generate a delayed clock signal; [[and]]

a multiplexer ~~comprising a non-delay line input, a delay line input and an output, wherein the multiplexer receives output directly from the non-delayed line and the delay line~~ having a first input adapted to receive the clock signal, a second input adapted to receive the delayed clock signal, and a third input used to selectively couple the first and second inputs to a multiplexer output; and

a state machine having an output coupled to the third input of the multiplexer, the state machine adapted to cause the multiplexer to ~~select either the non-delayed line or the delayed line~~ sequentially couple the first and second inputs to the multiplexer output.

2-3. (Cancelled).

4. (New) A method for generating a reduced amplitude clock pulse, the method comprising:

receiving a clock signal;

generating a delayed clock signal based on the clock signal;

providing a multiplexer having a first input adapted to receive the clock signal, a second input adapted to receive the delayed clock signal, and a third input used to selectively couple the first and second inputs to a multiplexer output; and

providing a state machine having an output coupled to the third input of the multiplexer, the state machine adapted to cause the multiplexer to sequentially couple the first and second inputs to the multiplexer output.